AMENDMENTS TO THE CLAIMS

1-67. (Canceled)

68. (Currently Amended) A method of forming a semiconductor transistor, comprising:

forming a first gate dielectric over a substrate;

forming a first ~~type~~ conductive gate region over said first gate dielectric;

forming a dielectric layer on the sides of said first ~~type~~ conductive gate region;

forming a second gate dielectric over said substrate;

forming a second ~~type~~ conductive gate region over said second gate dielectric, adjacent to said dielectric layer, and on the sides of said first ~~type~~ conductive region; and

forming source and drain regions in said substrate to define a channel region between them and beneath said first and second conductive type gate regions,

wherein all portions of said first gate dielectric, first ~~type~~ conductive gate region, second gate dielectric, and second ~~type~~ conductive gate region are wholly between said source and drain regions.

69. (Currently Amended) The method of claim ~~69~~ 92, wherein said first ~~type~~ conductive region is of P+ conductivity type and said second ~~type~~ conductive region is of N+ conductivity type.

70. (Original) The method of claim 69, wherein the act of forming said P+ type conductive region comprises:

forming said P+ type conductive region over said first gate dielectric;

forming a conductive material region over said P+ type conductive region;

forming a protective cap over said conductive material region; and

removing a portion of said P+ type conductive region, said conductive material region and said protective cap by etching, using said first gate dielectric as a stop to leave a freestanding vertical portion of said P+ type conductive region, said conductive material region and said protective cap.

71. (Original) The method of claim 70, wherein the act of forming said dielectric layer comprises forming a layer comprising a material selected from the group consisting of nitride, ox nitride, and nitrided oxynitride, on the sides of said P+ type conductive layer.

72. (Original) The method of claim 71, wherein the act of forming the N+ type conductive region comprises:

forming a region of N+ type conductive material over said second gate dielectric and adjacent to said dielectric layer and said P+ type conductive region; and

removing a portion of said N+ type conductive region to leave substantially vertical portions of said N+ type conductive region adjacent to and on the sides of said P+ type conductive region, wherein said dielectric layer separates said substantially vertical portions of said N+ type conductive region from said P+ type conductive region.

73. (Original) The method of claim 72, further comprising forming a conductive cap over said substantially vertical portions of said N+ type conductive region and said P+ type conductive region.

74. (Original) The method of claim 73, further comprising forming electrically insulating sidewalls adjacent to said conductive cap and said substantially vertical portions of said N+ type conductive region.

75. (Original) The method of claim 74, further comprising performing an ion implant to form source and drain regions in said substrate.

76. (Original) The method of claim 75, wherein said P+ type conductive region is formed to a thickness of up to about 200 nm.

77. (Original) The method of claim 76, wherein said P+ type conductive region comprises doped polysilicon.

78. (Original) The method of claim 76, wherein said P+ type conductive region comprises silicon-germanium.

79. (Original) The method of claim 76, wherein said P+ type conductive region comprises silicon carbide.

80. (Original) The method of claim 76, wherein said P+ type conductive region comprises silicon oxycarbide.

81. (Original) The method of claim 75, wherein said dielectric layer is up to about 2.0 nm thick.

82. (Original) The method of claim 81, wherein said dielectric layer comprises nitride.

83. (Original) The method of claim 75, wherein said N+ type conductive region is up to about 50 nm thick.

84. (Original) The method of claim 83, wherein said N+ type conductive region comprises doped polysilicon.

85. (Original) The method of claim 83, wherein said N+ type conductive region comprises silicon carbide.

86. (Original) The method of claim 83, wherein said N+ type conductive region comprises silicon oxycarbide.

87. (Original) The method of claim 75, wherein said conductive cap is up to about 100 nm thick.

88. (Original) The method of claim 87, wherein said conductive cap comprises polysilicon.

89. (Currently amended) A method of forming a semiconductor transistor, comprising:

providing a substrate;

forming a first gate dielectric layer over said substrate;

forming a P+ type conductive layer over said first gate dielectric;

selectively etching said P+ type conductive layer to leave at least two substantially vertical P+ type conductive layer regions over said first gate dielectric;

removing a portion of said first gate dielectric by selectively etching to said substrate to leave said at least two substantially vertical P+ type conductive layer regions over remaining said first gate dielectric;

forming a nitride layer on the sidewalls of each of said P+ type conductive layer regions;

forming a second gate dielectric over said substrate;

forming a N+ type conductive layer over said second gate dielectric and adjacent to said nitride layer and on the sides of each said substantially vertical P+ type conductive layer region;

etching said N+ type conductive layer to leave at least two structures, said at least two structures including the substantially vertical P+ type conductive layer regions and the adjacent regions of the N+ type conductive layer, said nitride layer separating said N+ type conductive layer regions from said P+ type conductive layer regions;

forming a conductive cap over each of said at least two structures; and

forming insulating sidewalls adjacent to said N+ type regions and said conductive caps.

90. (Currently Amended) A method of forming a semiconductor transistor, comprising:

providing a substrate;

forming a first gate dielectric layer over said substrate;

forming a first gate electrode over said first gate dielectric layer, said first gate electrode having a first workfunction and sidewalls;

forming a dielectric layer on the sidewalls of said first gate electrode;

forming a second gate dielectric layer over said substrate;

forming a pair of second gate electrodes over said second gate dielectric and adjacent to said dielectric layer, said second gate electrodes being separated from said first gate electrode by said dielectric layer, said pair of second gate electrodes having a second workfunction which is different than said first workfunction;

forming a conductive cap over each of said gate electrodes;

forming insulating sidewalls adjacent to said conductive cap and said gate electrodes; and

forming source and drain regions in said substrate to define a channel region between them and beneath said first and second conductive type gate regions,

wherein all portions of said first gate dielectric layer, first ~~type conductive~~ gate ~~region~~ electrode, second gate dielectric layer, and pair of second ~~type conductive~~ gate ~~region~~ electrodes are wholly between said source and drain regions.

91. (Original) The method of claim 90, wherein said second workfunction is more negative than said first workfunction.

92. (New) The method of claim 68, wherein said first and second conductive gate regions have different conductivity types.

93. (New) The method of claim 68, further comprising forming first and second gate contacts capable of independently biasing said first and second conductive gate regions.

94. (New) The method of claim 68, wherein said second conductive gate region is capable of forming at least one of virtual source and drain regions when receiving a bias voltage.

95. (New) The method of claim 68, wherein said second gate dielectric is thinner than said first gate dielectric.

96. (New) The method of claim 90, wherein said first gate electrode and said pair of second gate electrodes have different conductivity types.

97. (New) The method of claim 90, further comprising forming first and second gate contacts capable of independently biasing said first gate electrode and said pair of second gate electrodes.

98. (New) The method of claim 90, wherein said pair of second gate electrodes are capable of forming respective virtual source and drain regions when receiving a bias voltage.

99. (New) The method of claim 90, wherein said second gate dielectric layer is thinner than said first gate dielectric layer.

100. (New) A method of forming a semiconductor transistor, comprising:

forming source and drain regions defining a channel region therebetween; and

forming first and second gate regions capable of being independently biased, said second gate region forming at least one of virtual source and drain regions when receiving a bias voltage.

101. (New) The method of claim 100, wherein said first and second gate regions have different conductivity types.

102. (New) The method of claim 101, further comprising forming first and second gate dielectrics respectively insulating said first and second gate regions from said channel region, said first gate dielectric being thicker than said second gate dielectric.